

General Description

In applications with microprocessors (μ Ps) that have a RESET input, the MAX7705 is functionally and socket compatible with the TL7705, but requires **no external components.** It provides power-supply glitch immunity and a guaranteed power-up reset delay, while typically consuming $1/27^{th}$ the power from a +5V supply.

The MAX7705 monitors the power supply in μP and digital systems. The $\overline{\mbox{RESET}}$ output is valid for V_{CC} down to 1V. The device offers excellent circuit reliability and low cost by eliminating external components and adjustments.

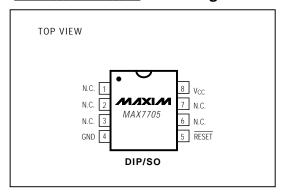
A system reset is provided during power-up, power-down, and brownout conditions. When V_{CC} is below the reset threshold, $\overline{\mbox{RESET}}$ is low and holds the μP in reset. $\overline{\mbox{RESET}}$ will go high 280ms after V_{CC} rises above the reset threshold. The MAX7705 is available in 8-pin DIP and SO packages.

| FEATURE | | MAX7705 | TL7705 |
|-------------------------------------|-----|---------|--------|
| No. of External Components Requi | red | 0 | 3 |
| Operating Supply | +5V | 65μΑ | 1.8mA |
| Current | +3V | 35μΑ | 1.8mA |
| Power-Supply Glitch Immunity | | Yes | No |
| Guaranteed Minimu Reset Delay | ım | Yes | No |

Applications

Minimum Component Count, Low-Cost Processor Systems

Pin Configuration



MIXIM

Features

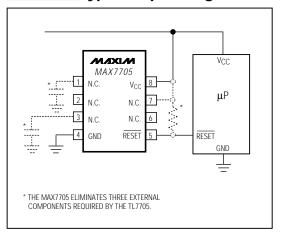
- **♦ No External Components**
- **♦ Low Cost**
- **♦ Precise Reset Threshold**
- ♦ 280ms Power-On Reset Delay
- ♦ 8-Pin DIP and SO Packages

Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
|------------|----------------|---------------|
| MAX7705CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX7705CSA | 0°C to +70°C | 8 SO |
| MAX7705C/D | 0°C to +70°C | Dice* |
| MAX7705EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX7705ESA | -40°C to +85°C | 8 SO |
| | | |

^{*} Contact factory for dice specifications.

Typical Operating Circuit



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MAX7705

μP Power-Supply Monitor with Reset

ABSOLUTE MAXIMUM RATINGS

| Terminal Voltage (with respect to GND) | |
|---|-----------------------------|
| V _{CC} | 0.3V to 6.0V |
| RESET | $0.3V$ to $(V_{CC} + 0.3V)$ |
| Input Current, VCC | 20mA |
| Output Current, RESET | 20mA |
| Rate-of-Rise, VCC | 100V/µs |
| Continuous Power Disipation (TA = +70°C | :) |
| Plastic DIP (derate 9.09mW/°C above + | -70°C)727mW |
| SO (derate 5.88mW/°C above +70°C) | 471mW |

| 0°C to +70°C |
|----------------|
| 40°C to +85°C |
| 65°C to +160°C |
| c)+300°C |
| |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

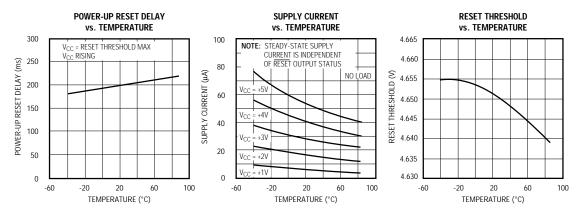
(V_{CC} = full range, T_A = T_{MIN} to T_{MAX} , unless otherwise noted.)

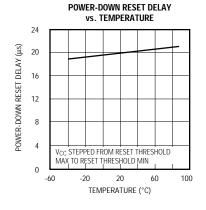
| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------|--|-----------------------|------|------|-------|
| Vee Dange | MAX7705C | 1.0 | | 5.5 | V |
| V _{CC} Range | MAX7705E | 1.2 | | 5.5 | V |
| Cupply Current | MAX7705C, V _{CC} < 5.5V | | 65 | 150 | μА |
| Supply Current | MAX7705E, V _{CC} < 5.5V | | 65 | 200 | |
| RESET Threshold | | 4.50 | 4.65 | 4.75 | V |
| V _{CC} to RESET Delay | V _{CC} = reset threshold max to reset threshold min | | 20 | | μs |
| Reset Active Timeout Period | V _{CC} = reset threshold max, V _{CC} rising | 140 | 280 | 560 | ms |
| | I _{SINK} = 3.2mA, V _{CC} = reset threshold min | | | 0.4 | |
| RESET Output Voltage | I _{SINK} = 50μA, V _{CC} ≥ 1.0V, MAX7705C | | | 0.3 | |
| neger Output Voltage | I _{SINK} = 100μA, V _{CC} ≥ 1.2V, MAX7705E | | | 0.4 | ٧ |
| | I _{SOURCE} = 800μA, V _{CC} ≥ reset threshold max | V _{CC} - 1.5 | | | 1 |

μΡ Power-Supply Monitor with Reset

_Typical Operating Characteristics

 $(T_A = +25^{\circ}C, \text{ unless otherwise noted.})$





Pin Description

| PIN | NAME | FUNCTION |
|-----------|-------|---|
| 1,2,3,6,7 | N.C. | No Connection. There is no internal connection to these pins. |
| 4 | GND | Ground |
| 5 | RESET | Reset Output remains low while V_{CC} is below the reset threshold, and for 280ms after V_{CC} rises above the reset threshold. |
| 8 | Vcc | +5V Supply Voltage |

µP Power-Supply Monitor with Reset

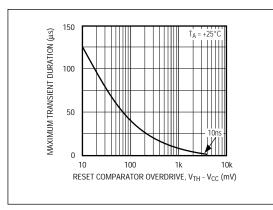


Figure 1. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

_Applications Information

Replacing the TL7705 with a MAX7705 in an Existing Design

The MAX7705 has only three active pins: V_{CC} , GND, and RESET. When using a TL7705 with a μP that has a RESET input, simply plug the MAX7705 into the same socket and omit the RESET pull-up resistor, reset timing capacitor, and reference bypass capacitor (see the Typical Operating Circuit).

The MAX7705 monitors the V_{CC} voltage and asserts reset whenever V_{CC} falls below the reset threshold. The reset power-up delay is created by an internal fixed oscillator. This delay is 100% tested and guaranteed over the full temperature range. The RESET output both sources and sinks current (see RESET Output Voltage in the *Electrical Characteristics*).

Negative-Going VCC Transients

The MAX7705 asserts $\overline{\text{RESET}}$ during power-up, power-down, and brownout conditions. However, it is relatively immune to short-duration negative-going V_{CC} transients (glitches).

Figure 1 shows typical transient duration vs. reset comparator overdrive for which the MAX7705 does **not** generate a reset pulse. The graph was generated using a fast-edge, negative-going pulse applied to $V_{\rm CC}$, starting 1.5V above the actual reset threshold and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). It indicates the typical maximum actions the starting transition of the starting transition of

mum pulse width a negative-going V_{CC} transient may have without causing a reset pulse to be issued. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 40 μ s or less will not cause a reset pulse to be issued.

A 0.1 μF bypass capacitor mounted as close as possible to pin 2 (V $_{CC}$) provides additional transient immunity.

Ensuring a Valid \overline{RESET} Output Down to $V_{CC} = 0V$

When V_{CC} falls below 1V, the MAX7705 $\overline{\text{RESET}}$ output no longer sinks current; it becomes high impedance. Therefore, high-impedance CMOS logic inputs connected to the RESET output can drift to indeterminate voltages. In most applications this presents no problem, as μP and other circuitry is generally inoperative with V_{CC} below 1V. In applications where the RESET output must be valid down to 0V, adding a pull-down resistor to the RESET pin (as shown in Figure 2) will cause any stray leakage currents to flow to ground, holding RESET low. The resistance value of R1 is not critical. It should be about $100k\Omega$, which is large enough not to load RESET and small enough to pull RESET to ground.

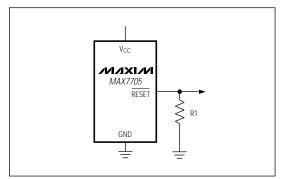


Figure 2. \overline{RESET} Valid to V_{CC} = Ground Circuit

μΡ Power-Supply Monitor with Reset

Interfacing to µPs with Bidirectional Reset Inputs

 μ Ps with bidirectional reset pins, such as Motorola's 68HC11 series, can contend with the MAX7705 reset output. If, for example, the MAX7705 **RESET** output is asserted high and the μ P wants to pull it low, an indeterminate logic level may result. To correct this, connect a 4.7k Ω resistor between the MAX7705 **RESET** output and the μ P reset I/O, as in Figure 3. Buffer the **RESET** signal to other system components.

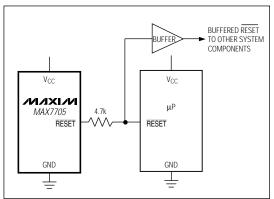
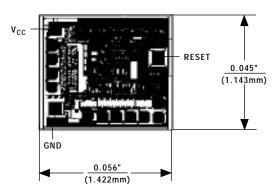


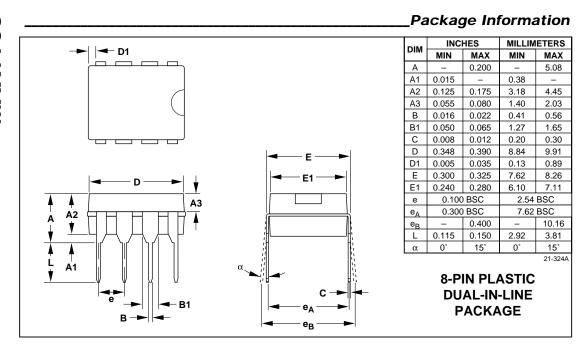
Figure 3. Interfacing to μPs with Bidirectional Reset I/O

_Chip Topography



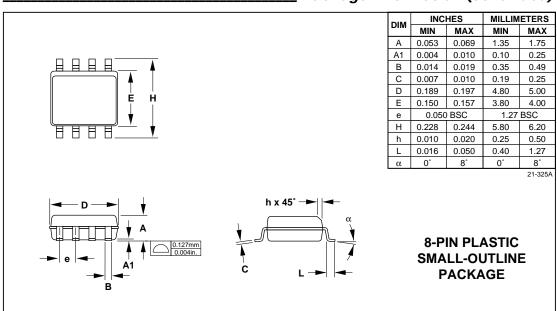
TRANSISTOR COUNT = 380; SUBSTRATE CONNECTED TO V_{CC} .

μP Power-Supply Monitor with Reset



μΡ Power-Supply Monitor with Reset

Package Information (continued)



MIXIM ——

μP Power-Supply Monitor with Reset

μ**P Supervisory Circuits**

| Part | Nominal Reset Threshold | Minimum Reset Pulse Width | Nominal Watchdog Timeout Period | Backup- Battery | CE - Write | Power- Fail Com- | Manual- Reset | Watch- dog | Low- Line | Active- High | Battery- On |
|---------------------|-------------------------------|------------------------------------|--|--------------------|----------------|------------------------|------------------|---------------|--------------|-----------------|----------------|
| Number | (V) | (ms) | (sec) | Switch | Protect | <u> </u> | Input | Output | Output | Reset | Output |
| MAX690A/692A | 4.65/4.40 | 140 | 1.6 | / | | / | | | | | |
| MAX691A/693A | 4.65/4.40 | 140/adj. | 1.6/adj. | ' | ✓ /10ns | ' | | ~ | ' | ~ | / |
| MAX696 | Adj. | 35/adj. | 1.6/adj. | ' | | ' | | ' | ' | ' | ' |
| MAX697 | Adj. | 35/adj. | 1.6/adj. | | ~ | ' | | ~ | ' | / | |
| MAX700 | 4.65/adj. | 200 | - | | | | v | | | v | |
| MAX703/704 | 4.65/4.40 | 140 | - | / | | ' | v | | | | |
| MAX705/706 | 4.65/4.40 | 140 | 1.6 | | | ' | v | v | | | |
| MAX706P | 2.63 | 140 | 1.6 | | | • | ~ | v | | ~ | |
| MAX706R/S/T | 2.63/2.93/ 3.08 | 140 | 1.6 | | | • | • | ~ | | | |
| MAX707/708 | 4.65/4.40 | 140 | - | | | ~ | ~ | | | ~ | |
| MAX708R/S/T | 2.63/2.93/ 3.08 | 140 | - | | | • | • | | | • | |
| MAX709L/M/ R/S/T | 4.65/4.40/ 2.63/2.93/3.08 | 140 | - | | | | | | | | |
| MAX791 | 4.65 | 140 | 1 | ~ | ✓ /10ns | • | v | ~ | • | ~ | <i>'</i> |
| MAX792L/M/ R/S/T | 4.65/4.40/ 2.63/2.93/3.08 | 140 | 1 | | ✓ /10ns | • | • | ~ | • | • | |
| MAX800L/M | 4.60/4.40 | 140 | 1.6/adj. | ~ | ✓ /10ns | ✓ /±2% | | ~ | • | ~ | / |
| MAX802L/M | 4.60/4.40 | 140 | 1.6 | ~ | | ✓ /±2% | | | | | |
| MAX805L | 4.65 | 140 | 1.6 | ~ | | • | | | | ~ | |
| MAX813L | 4.65 | 140 | 1.6 | | | • | v | ' | | ' | |
| MAX820L/M/ R/S/T | 4.65/4.40/ 2.63/2.93/3.08 | 140 | 1 | | ✓ /10ns | ✓ /±2% | • | ~ | • | • | |
| MAX1232 | 4.37/4.62 | 250 | 0.15/0.60/1.2 | | | | ~ | | | | |
| MAX1259 | - | - | - | ~ | | ~ | | | | <u> </u> | |

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